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PATENT & TRADEMARK OFFICE

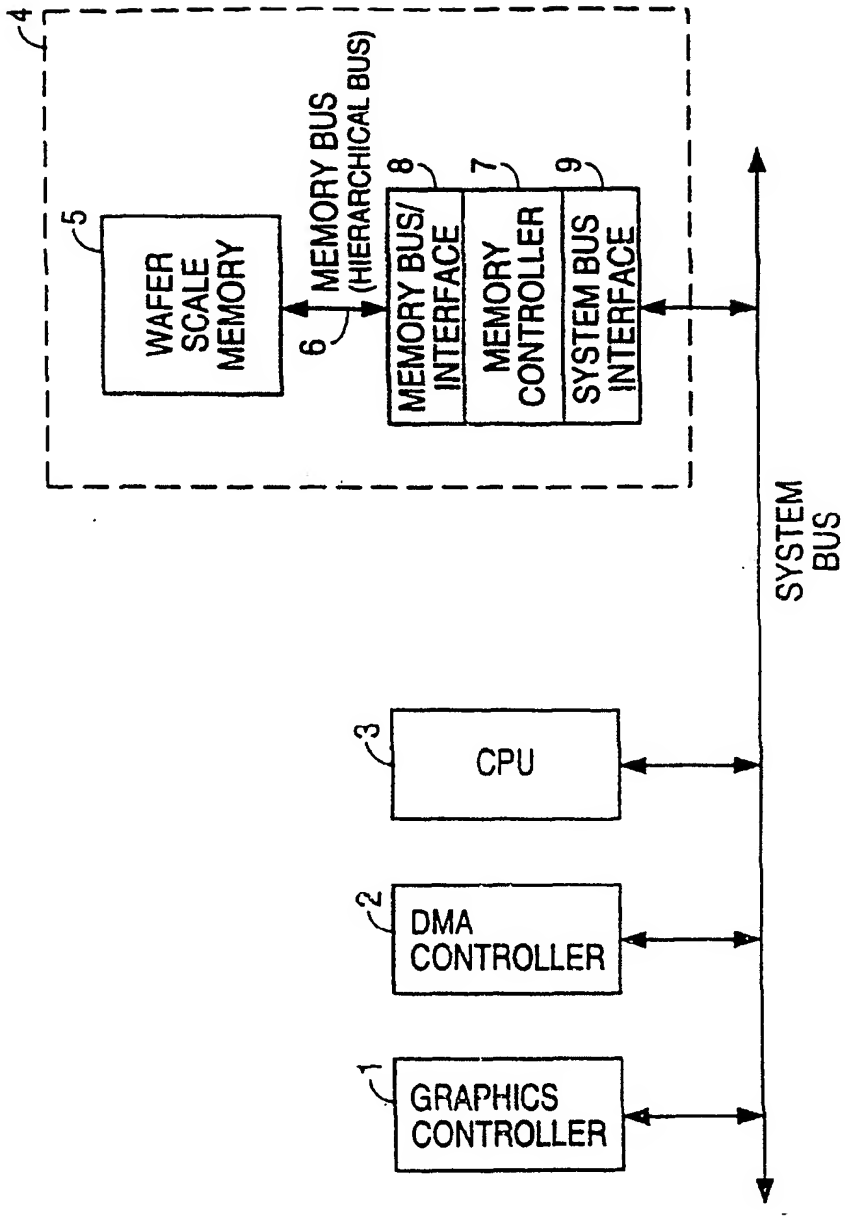

FIG. 1

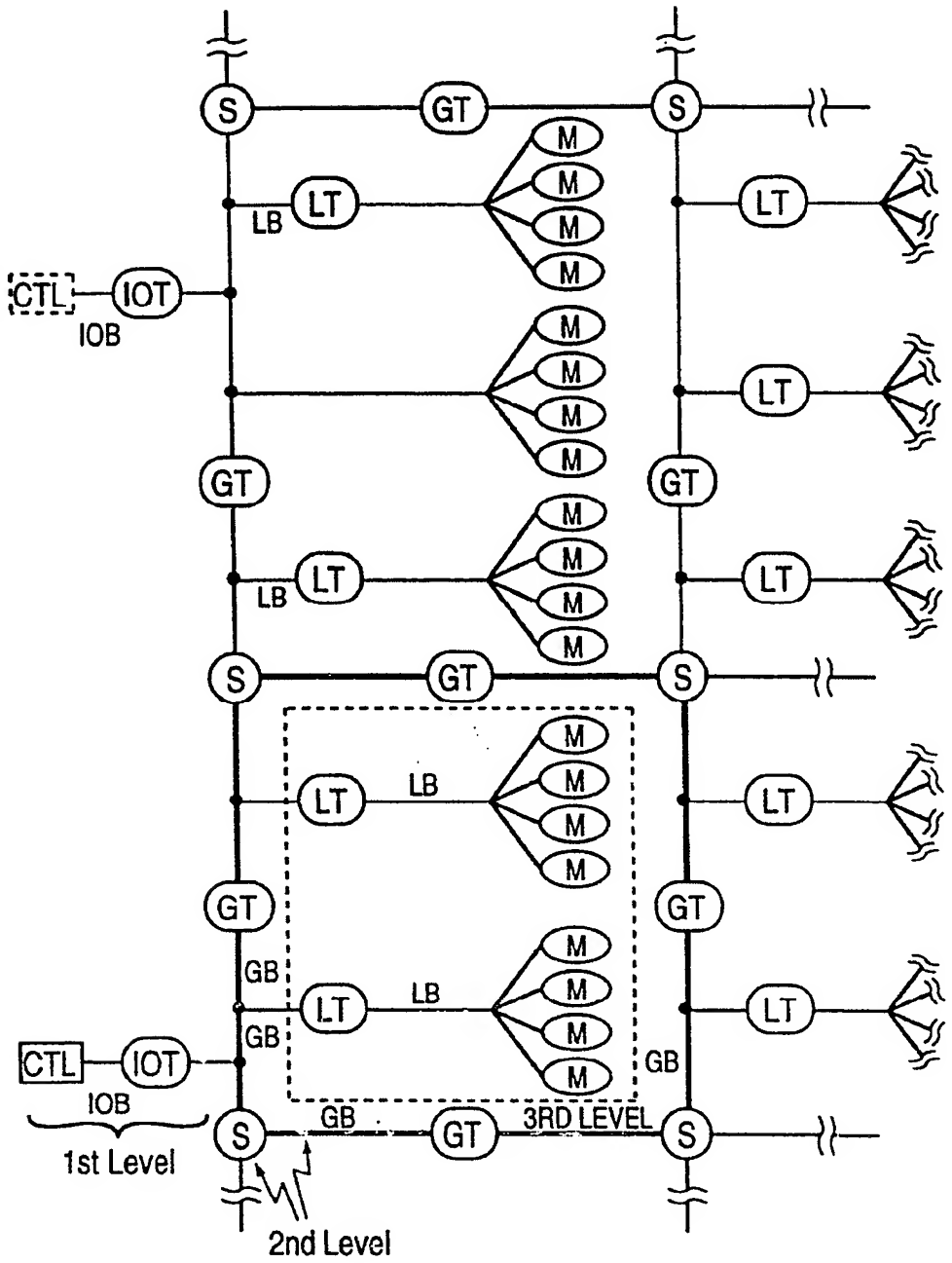
S
GT
M
LT
LB
CTL
IOT
IOB
GB
3RD LEVEL
1st Level
2nd Level
- Module
- Controller
- Possible Site for Controller

FIG. 2

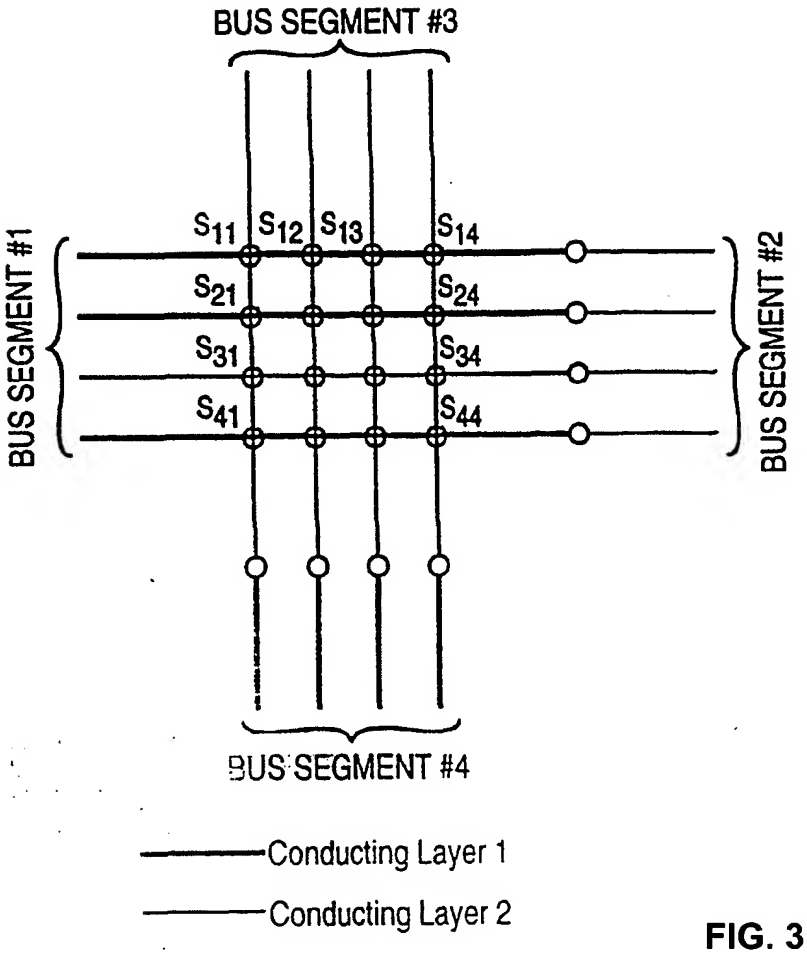

FIG. 3

Group 1 - Block - mode transfer signals

- Bus Data [0:8]
- Clk

Group 2 - Asynchronous control signals

- Bus Busy (BB#)
- Transmit / Receive (T / R)
- TriState Control (TC#)

FIG. 4

BB#	T/R	TC#	BUS STATE
0	0	0	Hi Z
0	0	1	Receive
0	1	0	Hi Z
0	1	1	Transmit
1	0	0	Idle
1	0	1	
1	1	0	
1	1	1	

FIG. 5

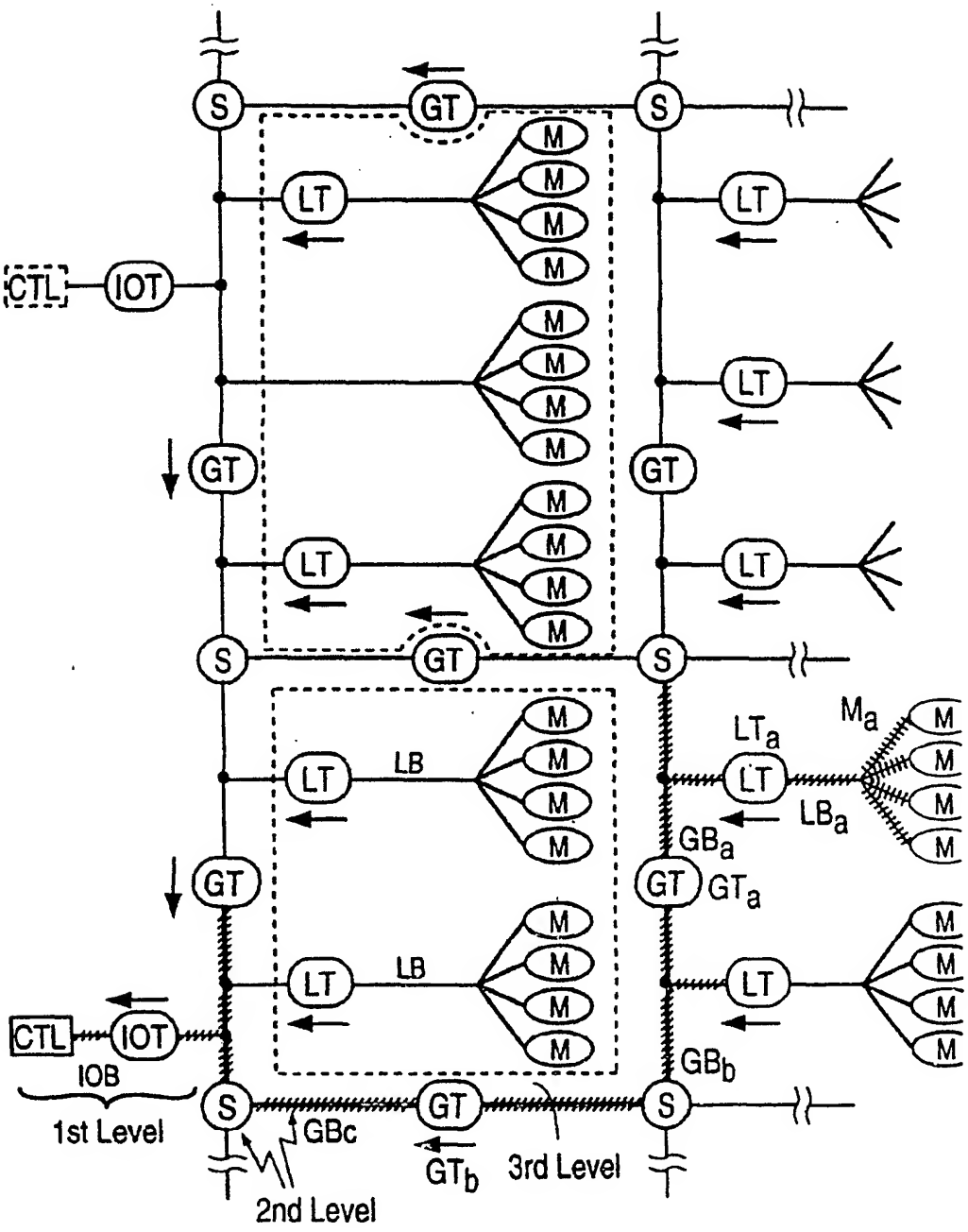
S
GT
LT
M
CTL
IOT
LB
LT_a
M_a
LB_a
GB_a
GT_a
GB_b
IOB
1st Level
GBc
GT_b
2nd Level
3rd Level
M - Module
CTL - Controller
CTL - Possible Site for Controller

FIG. 6

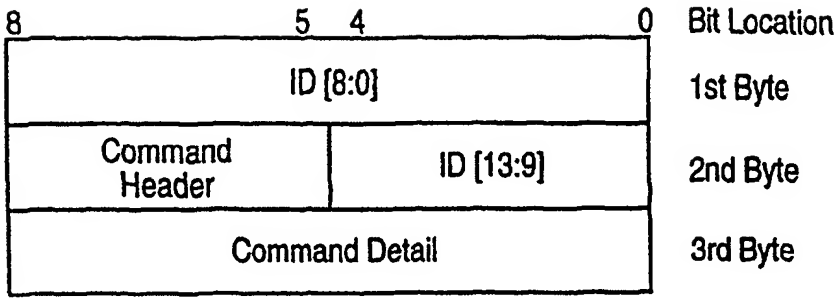
8
5
4
0
Bit Location
ID [8:0]
1st Byte
Command Header
ID [13:9]
2nd Byte
Command Detail
3rd Byte

FIG. 7

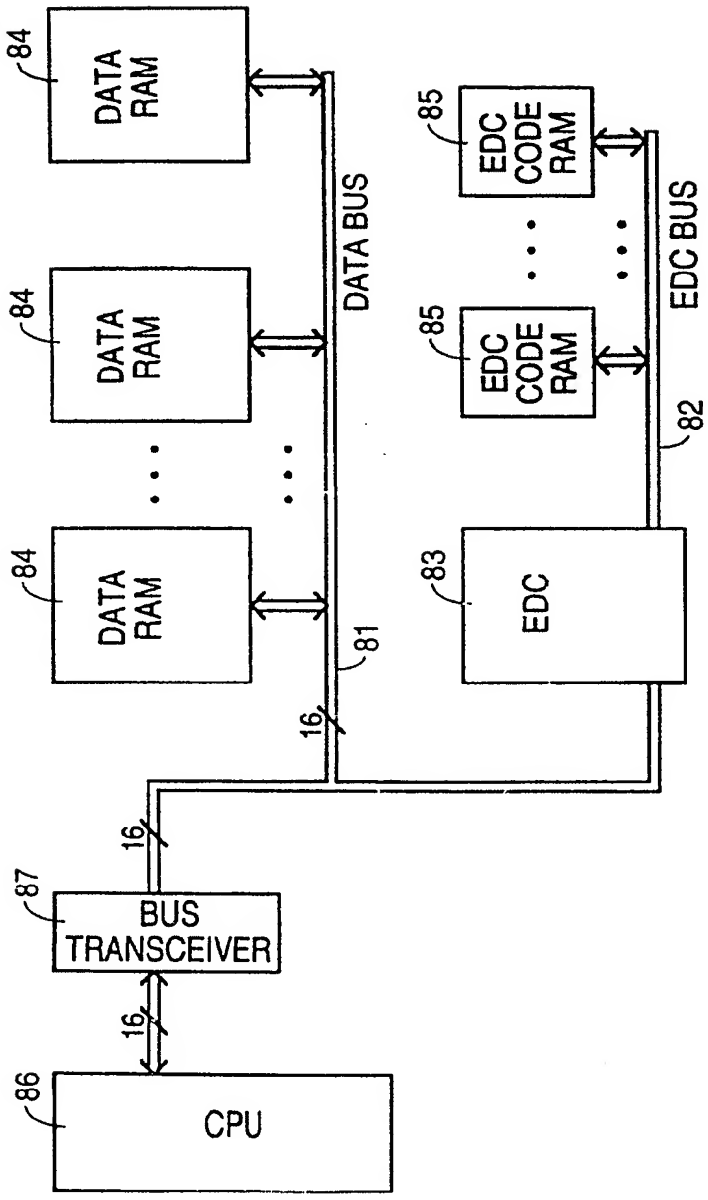
84
DATA RAM
84
DATA RAM
84
DATA RAM
DATA BUS
81
16
85
EDC CODE RAM
85
EDC CODE RAM
EDC BUS
82
83
EDC
16
87
BUS TRANSCEIVER
16
86
CPU

FIG. 8

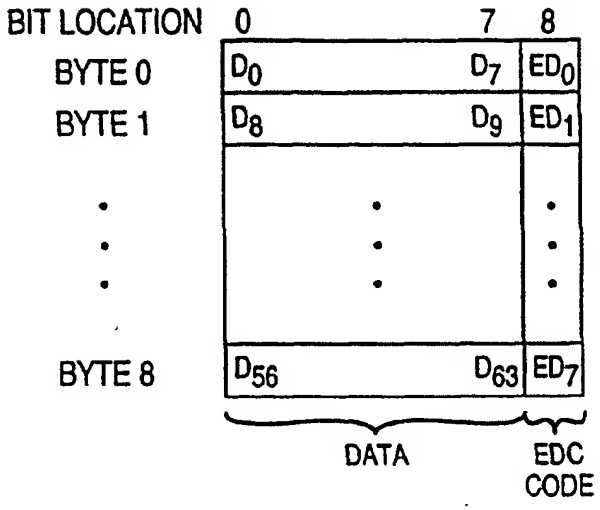
BIT LOCATION
0
7
8
BYTE 0
D0
D7
ED0
BYTE 1
D8
D9
ED1
BYTE 8
D56
D63
ED7
DATA
EDC CODE

FIG. 9

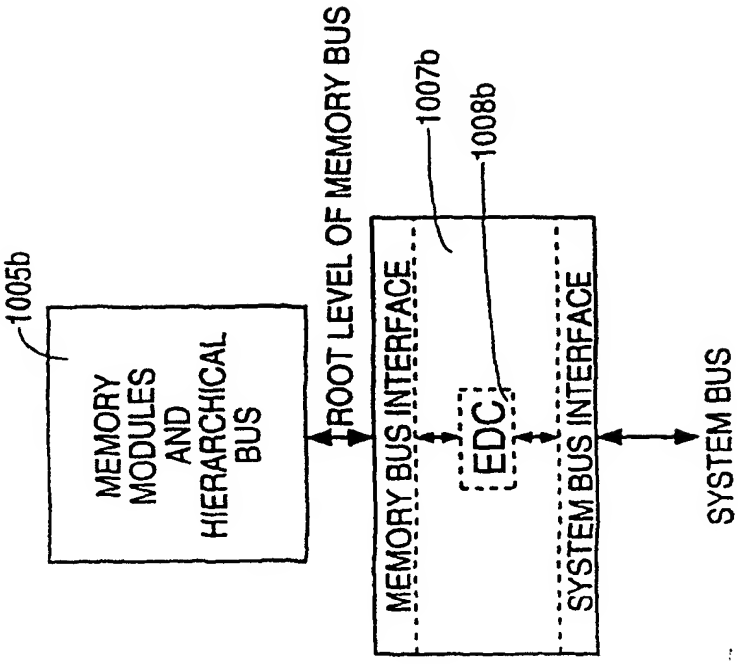

FIG. 10B

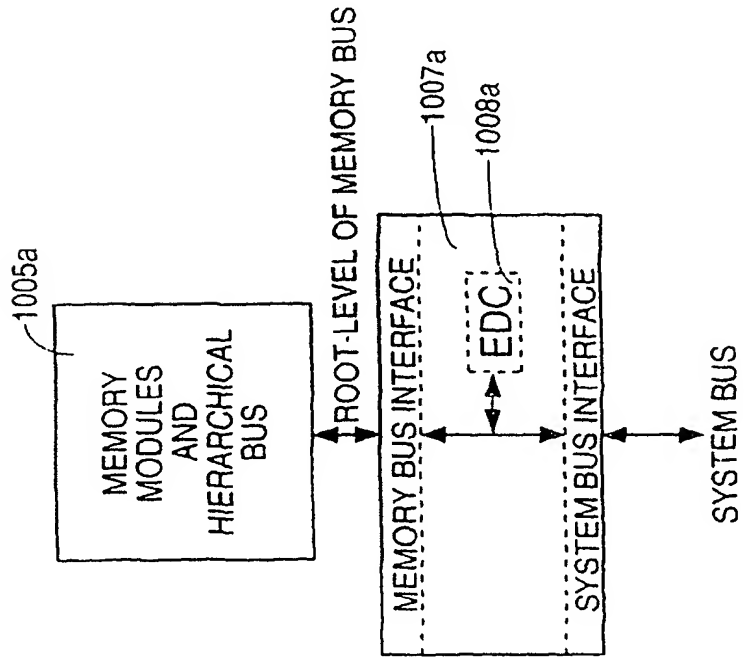

FIG. 10A

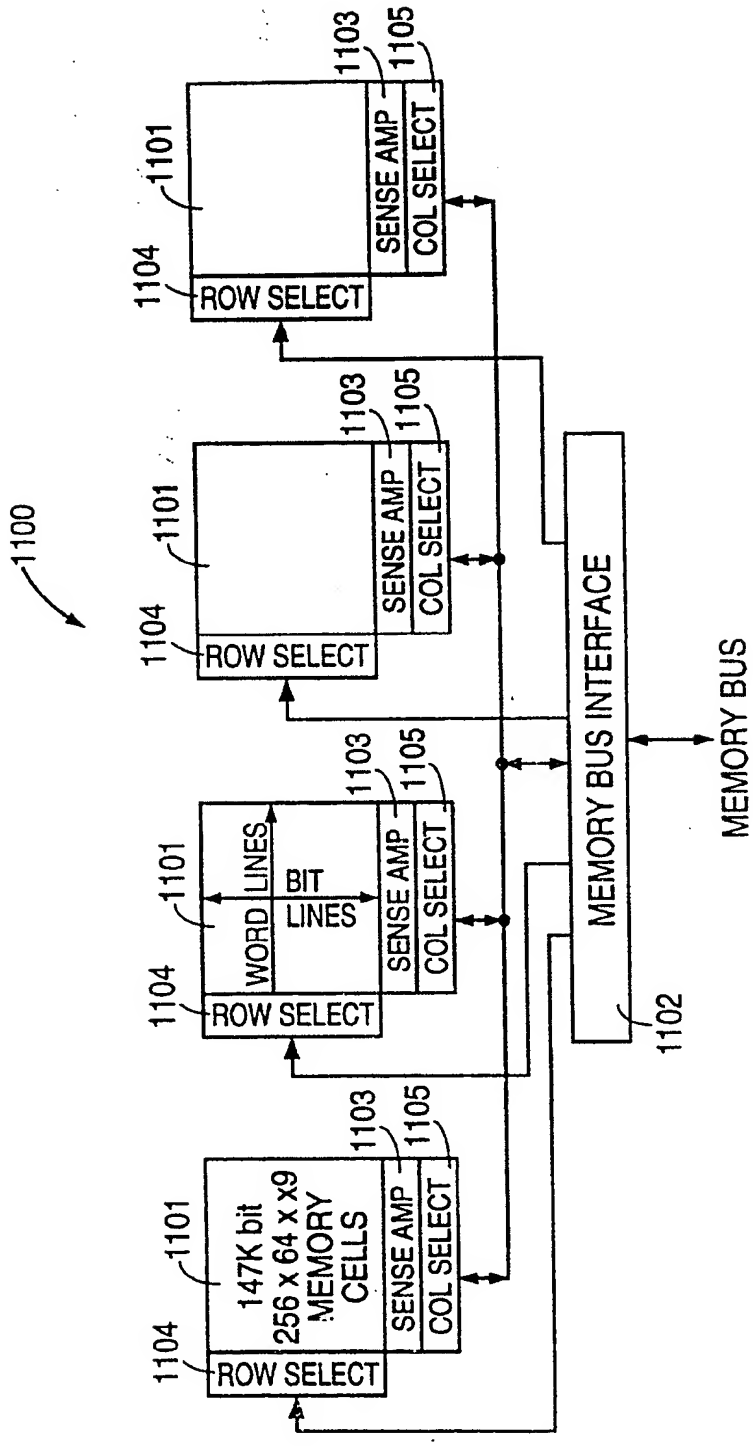
1100
1101
1103
1104
1105
ROW SELECT
SENSE AMP
COL SELECT
WORD LINES
BIT LINES
147K bit
256 x 64 x x9
MEMORY
CELLS
MEMORY BUS INTERFACE
MEMORY BUS
1102

FIG. 11

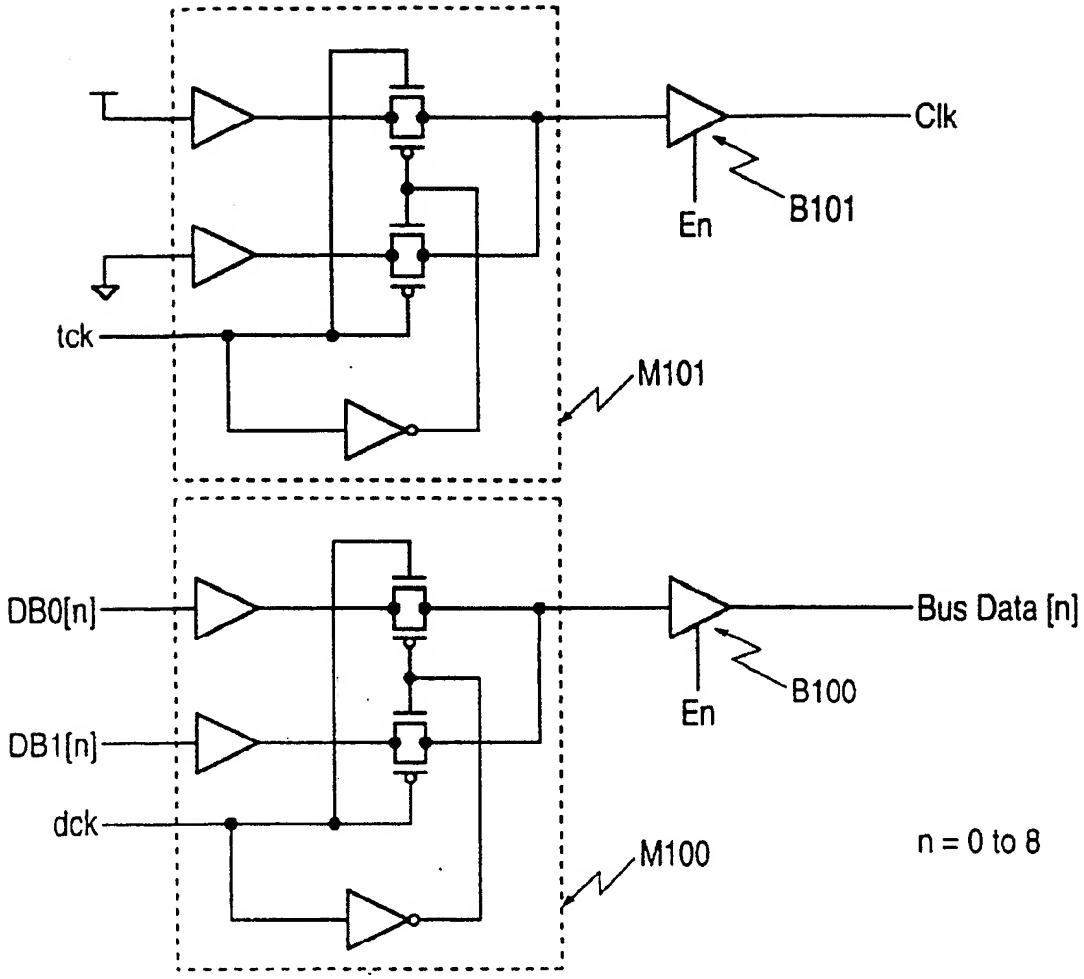

FIG. 12A

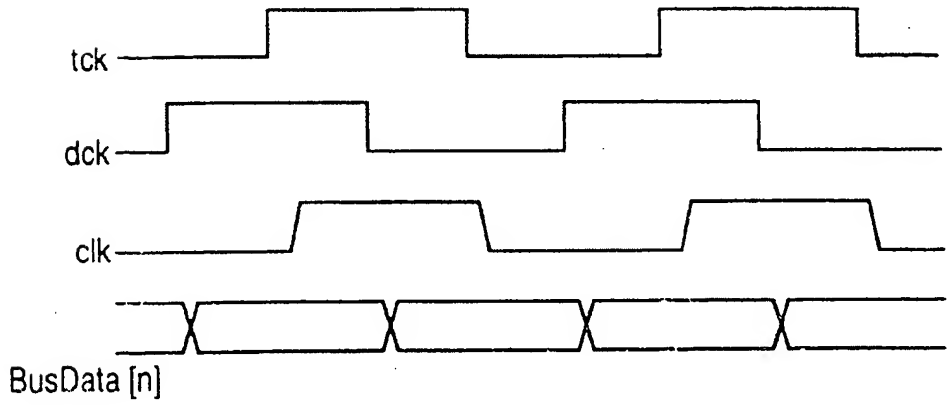

FIG. 12B

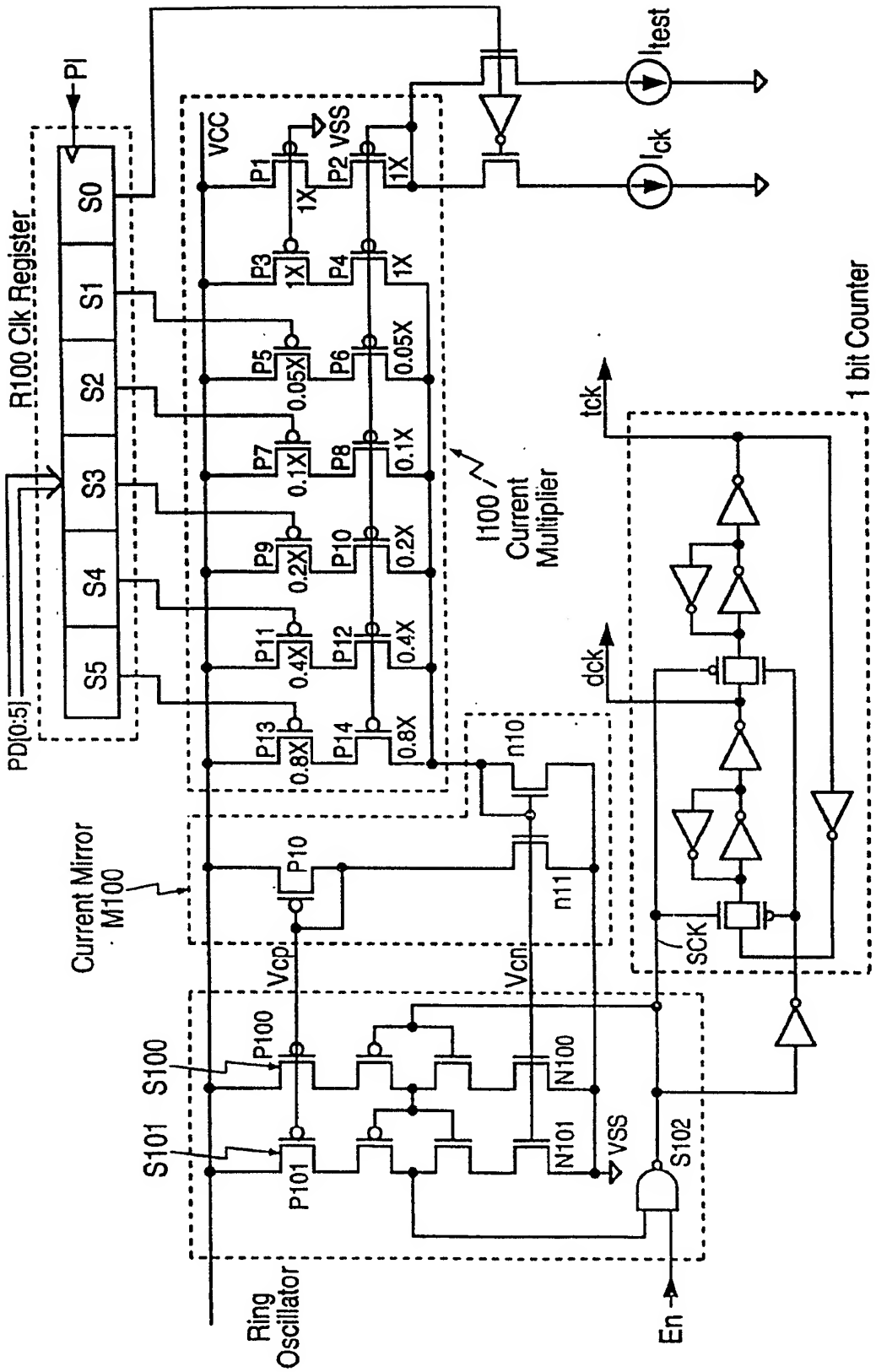
PI
R100 Clk Register
S0
S1
S2
S3
S4
S5
PD[0:5]
VCC
VSS
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
1X
0.05X
0.1X
0.2X
0.4X
0.8X
I100
Current
Multiplier
Itest
Ick
tck
dck
SCK
1 bit Counter
n10
n11
Current Mirror
M100
Vcp
Vcn
P100
N100
P101
N101
S100
S101
S102
VSS
Ring
Oscillator
En

FIG. 13

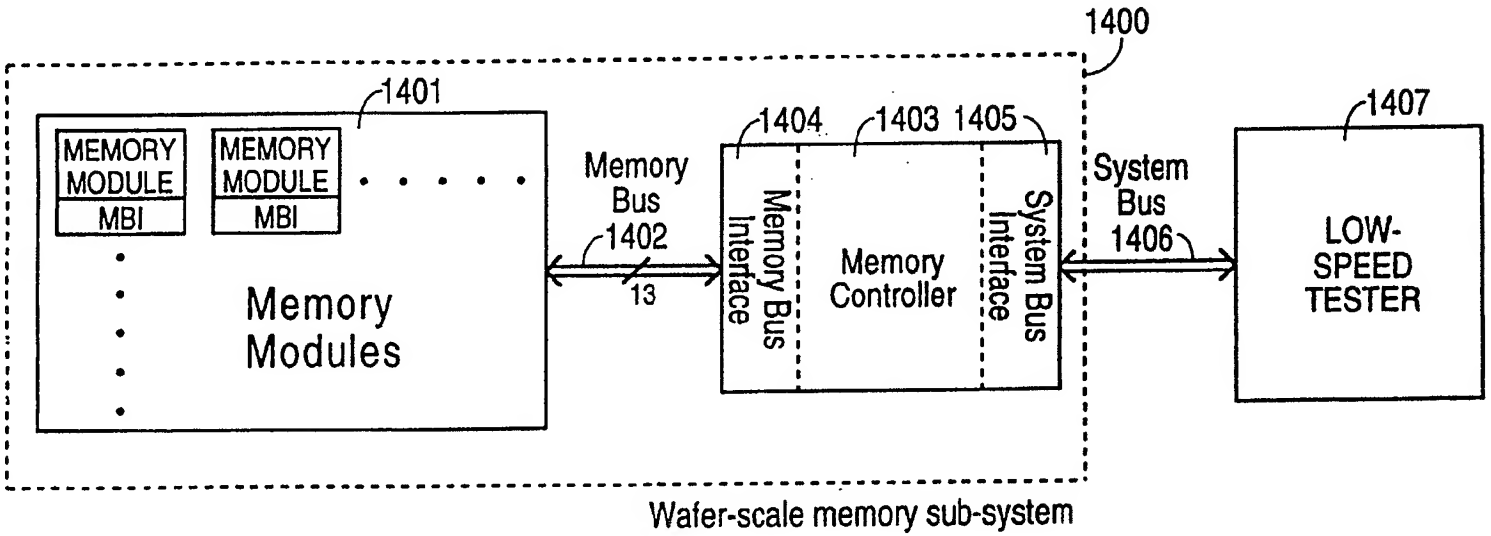

FIG. 14

MBI = Memory Bus Interface

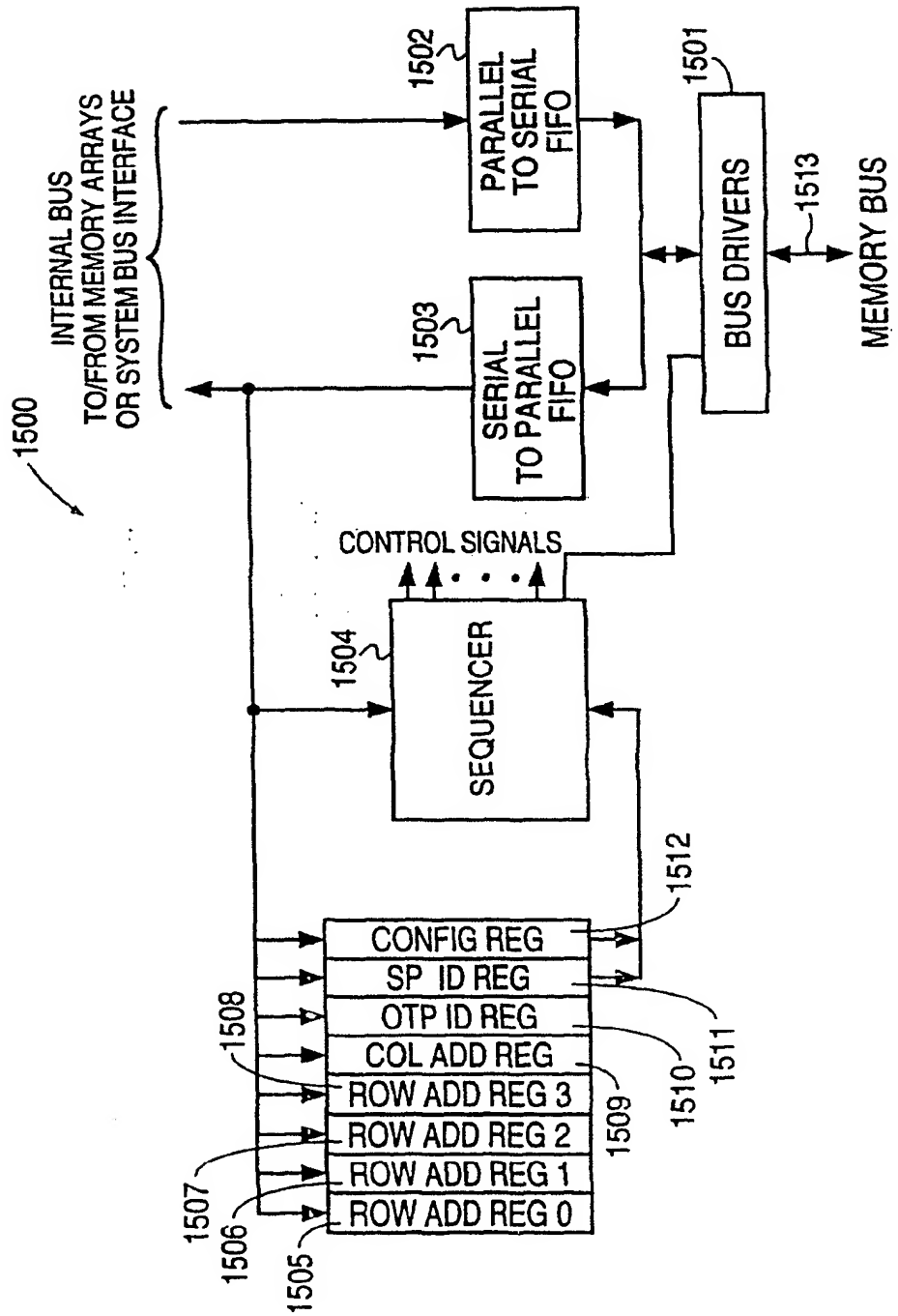
1500
INTERNAL BUS
TO/FROM MEMORY ARRAYS
OR SYSTEM BUS INTERFACE
1502
PARALLEL
TO SERIAL
FIFO
1503
SERIAL
TO PARALLEL
FIFO
1501
BUS DRIVERS
1513
MEMORY BUS
CONTROL SIGNALS
1504
SEQUENCER
1512
CONFIG REG
SP ID REG
OTP ID REG
COL ADD REG
ROW ADD REG 3
ROW ADD REG 2
ROW ADD REG 1
ROW ADD REG 0
1508
1507
1506
1505
1509
1510
1511

FIG. 15

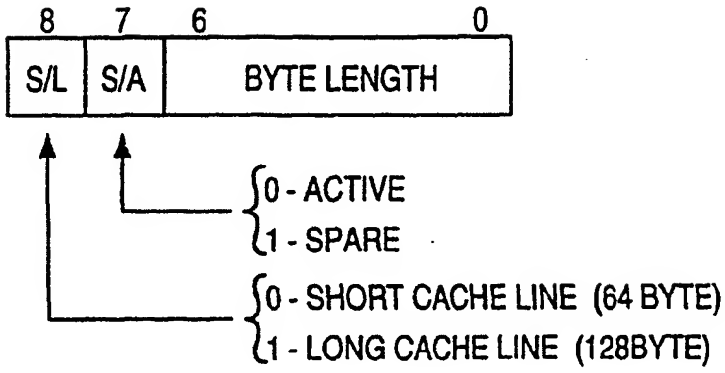
8
7
6
0
S/L
S/A
BYTE LENGTH
0 - ACTIVE
1 - SPARE
0 - SHORT CACHE LINE (64 BYTE)
1 - LONG CACHE LINE (128BYTE)

FIG. 16

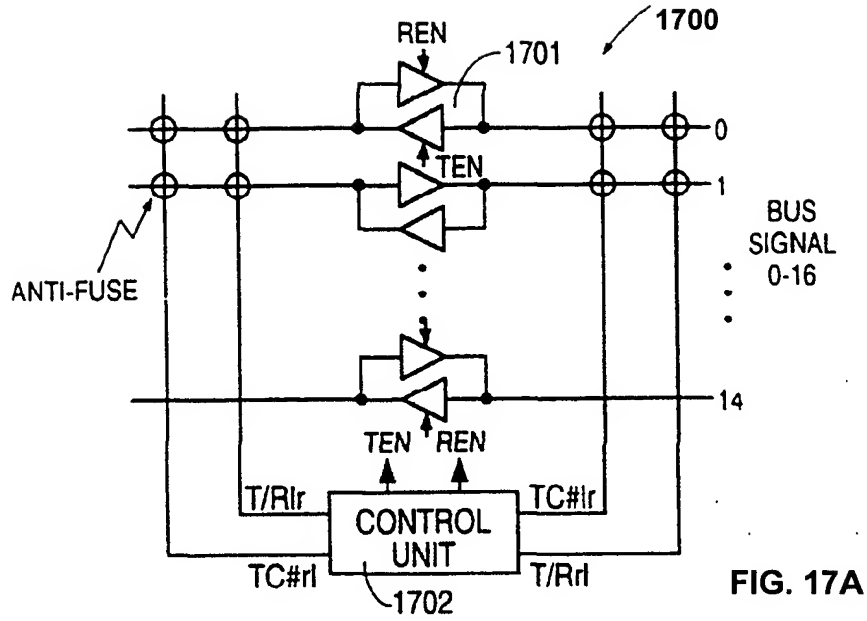

FIG. 17A

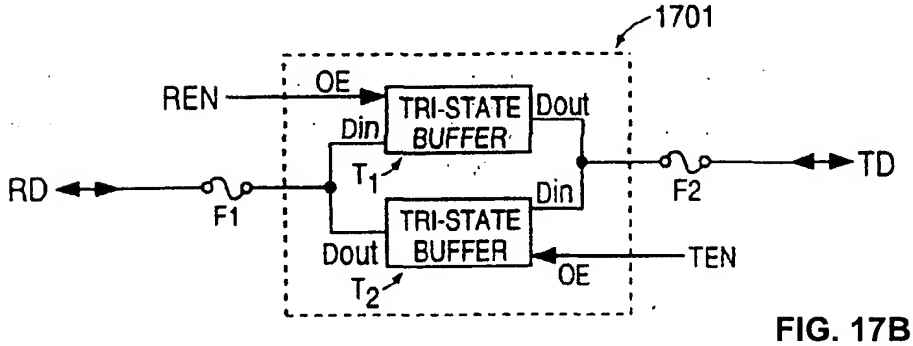

FIG. 17B

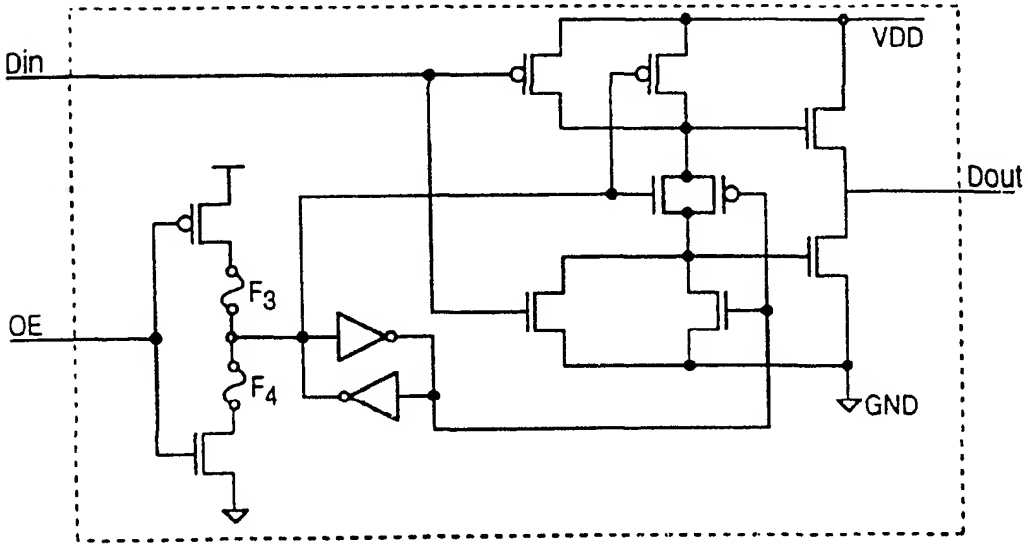

FIG. 17C

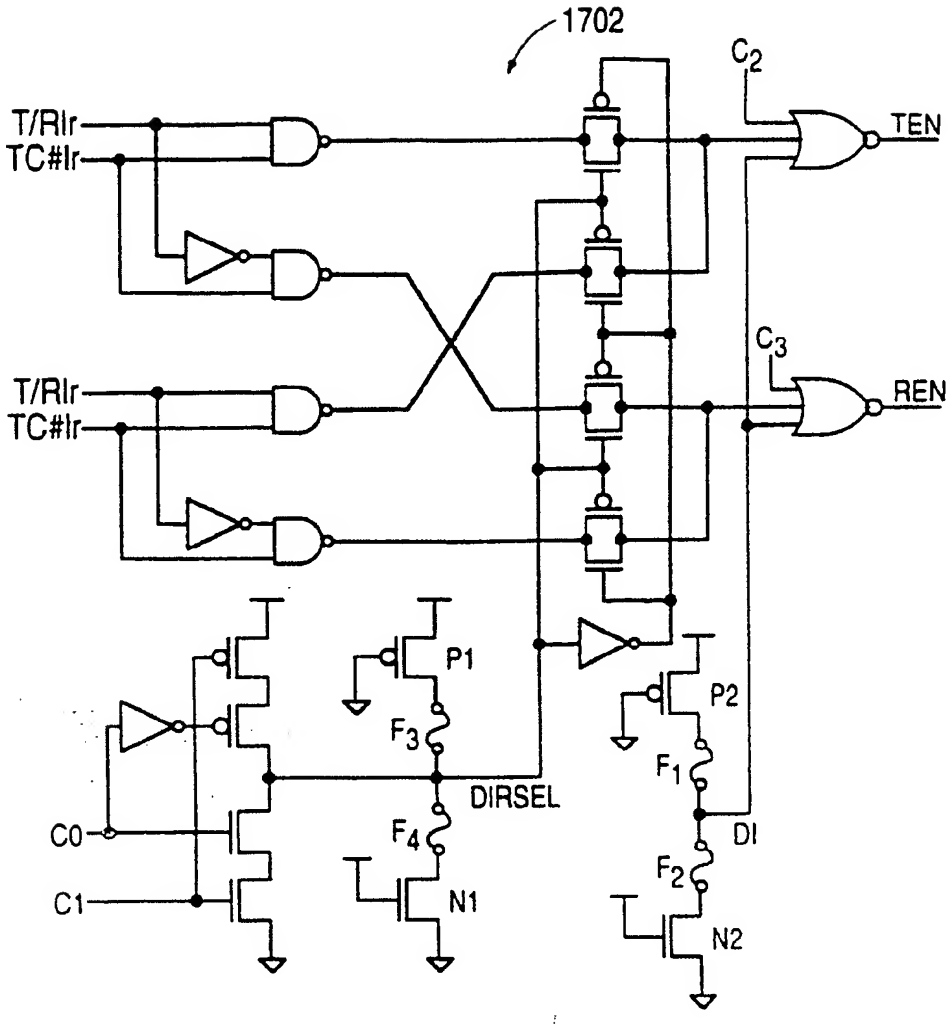

FIG. 17D

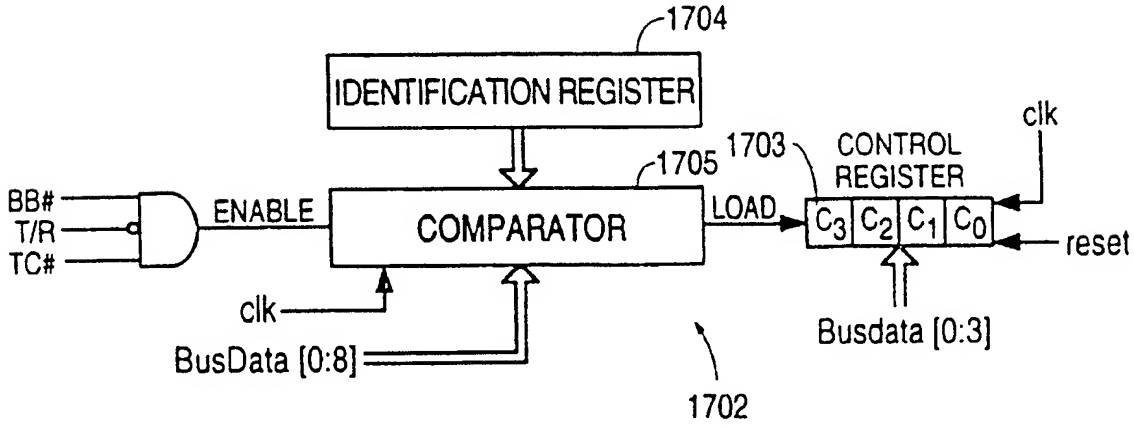

FIG. 17E

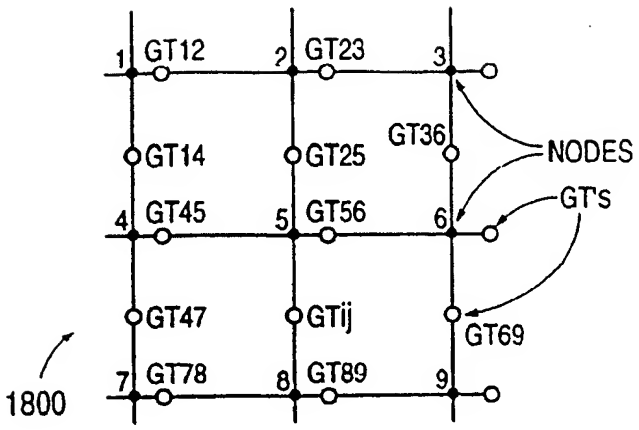

FIG. 18A

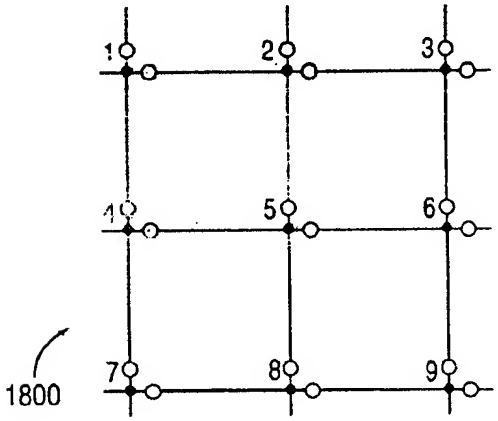

FIG. 18B

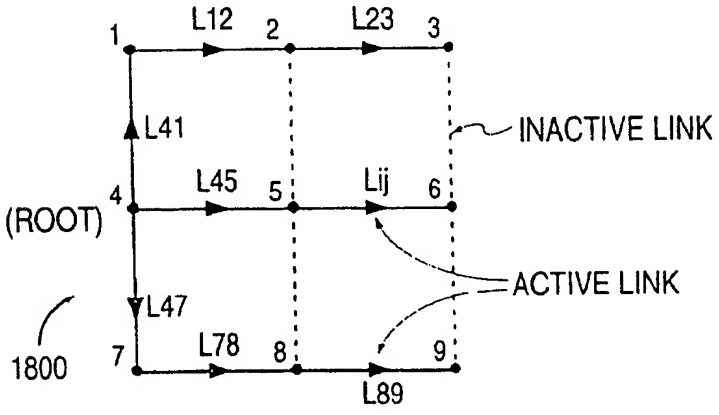

FIG. 18C

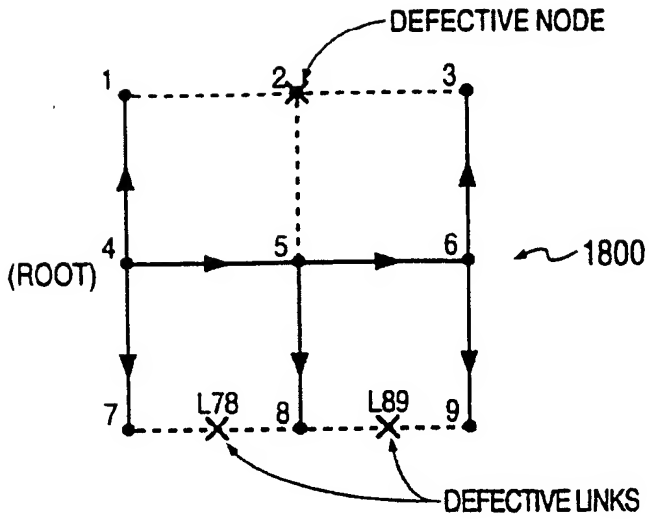

FIG. 18D

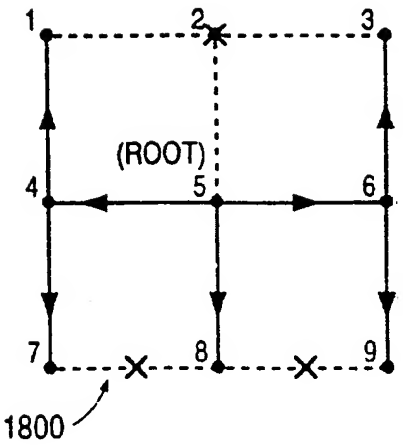

FIG. 18E

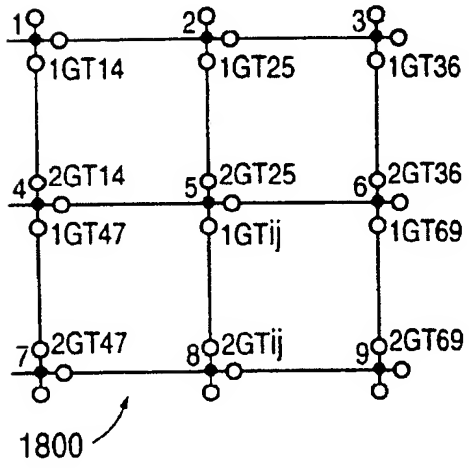

FIG. 18F

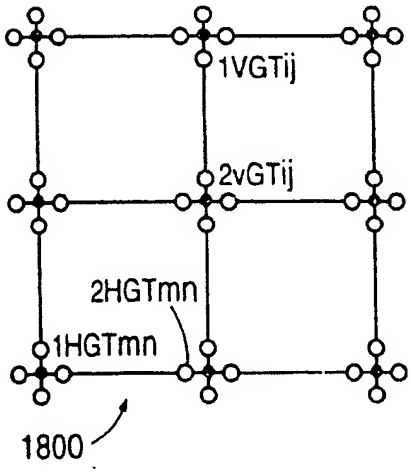

FIG. 18G